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10/671,132	09/25/2003	Jos Manuel Accapadi	AUS920030413US1	7286

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EXAMINER	
KAWSAR, ABDULLAH AL	

ART UNIT	PAPER NUMBER
2109	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,132	ACCAPADI ET AL.	
	Examiner	Art Unit	
	Abdullah-Al Kawsar	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/25/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/06/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 48 are pending.

Specification

2. The abstract of the disclosure is objected to because of the following informalities: in line 4 the word "CPI" should spell out. Appropriate correction is required. See MPEP § 608.01(b).

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 1 is objected to because of the following informalities: claim 1 "CPI" should spell out. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-4, 7, 8, 16-20, 23,24, 32-36, 39, 40 and 48 are rejected under 35 U.S.C. 102(a) as being anticipated by "Using Performance Reflection in Systems Software" by Robert Fowler (Fowler).

As per claim 1, Fowler discloses:

- A computer-implemented method of identifying compatible software threads to execute on an SMT processor, said method comprising (Page 1 col 1 lines 2-3, "performance monitoring counters in modern processors" and page 1 col 2 lines 2-3, "tuning of application code through compiler") inherently including a computer implemented method.

- identifying a time interval during which both a first thread and a second thread are executing on the SMT processor (page 2 col 1 lines 24-27, "the Cycles Per Instruction (CPI), which is a common measure of processor productivity, can be computed over some interval by taking the ratio of the number of cycles to the number of instructions graduated") where number of instruction are the first thread and second thread.

- retrieving a performance value that occurred during the identified time interval (page 2 col 1 lines 3-4, "We use these metrics to estimate productivity" and page 1 col 2 lines 24-26, "collect performance metrics using timers, event counters, and some programmed hooks") inherently including retrieving a performance value as claimed.

- determining, based upon the retrieved performance value, whether the first thread is compatible with the second thread; and recording the compatibility of the first thread with the second thread in response to the determination (page 2 col 2 lines "monitoring miss rates of the shared cache of a standard node would enable the system to either schedule only one thread per module or to possibly identify "compatible" threads to co-schedule.") where a compatible thread is a second thread.

As per claim 2, the rejection of claim 1 is incorporated and further Fowler discloses:

- wherein the performance value is a cycles per instruction (CPI) value (page 2 col 2 lines 35-37, "measuring remote references, cache miss behavior, or cycles per instruction (CPI)")

As per claim 3, the rejection of claim 2 is incorporated and further Fowler discloses:

- retrieving a number of cycles value indicating the number of processing cycles that occurred during the time interval; retrieving a number of instructions value indicating the number of instructions that were executed by the SMT processor during the time interval; and dividing the number of cycles value by the number of instructions value, the dividing resulting in the CPI value (page 2 col 1 lines 24-32, "the Cycles Per Instruction (CPI), which is a common measure of processor productivity, can be computed over some interval by taking the ratio of the number of cycles to the number of instructions graduated. While many different kinds of events can be counted, the number of distinct measures of productivity counted either by hardware counters or the OS is small, perhaps including instructions, FLOPs, and bytes/packets

transferred over I/O devices.") where estimating , measuring productivity inherently includes retrieving a number of cycles.

As per claim 4, the rejection of claim 2 is incorporated and further Fowler discloses:

- comparing the CPI value to a threshold value, wherein the first thread and second thread are determined to be compatible if the CPI value is better than the threshold value (page 1 col 1 lines 6-10, "In this paper we outline our approach of using these instrumentation mechanisms to estimate productivity and overhead metrics while running user applications. At the kernel level, we speculate that the scheduler can exploit these metrics to improve system performance") where matrices has the compared CPI value and compared with the scheduled value (threshold).

As per claim 7, the rejection of claim 5 is incorporated and further Fowler discloses:

- comparing the CPI value to one or more previously recorded CPI values that correspond to one or more previously identified compatible threads; and determining that the CPI value is better than at least one of the previously recorded CPI values (page 2 col 2 lines 35-37, "The kernel can monitor memory behavior by, depending on the level of architectural support, measuring remote references, cache miss behavior, or cycles per instruction (CPI). Thread rescheduling decisions can then be based on this feedback" and lines 40-41, "Applications can use the overhead and productivity metrics provided by the kernel, as well as application-specific productivity metrics to reactively change their policies")

As per claim 8, the rejection of claim 7 is incorporated and further Fowler discloses:

- removing one of the previously recorded CPI values and data corresponding to one of the previously identified compatible threads prior to the writing (Page 2 col 2 lines 40-41, "Applications can use the overhead and productivity metrics provided by the kernel, as well as application-specific productivity metrics to reactively change their policies") using the metrics to update policy means updating/replacing old values with the new values.

As per claim 16, the rejection of claim 14 is incorporated and further Fowler discloses:

- checking whether the compatible threads are ready to execute in order of a CPI value, wherein the compatible threads are checked in an order determined by a CPI value corresponding to each of the compatible threads, so that compatible threads with better CPI values are checked first. (page 2 col 1 lines 24-27, "the Cycles Per Instruction (CPI), which is a common measure of processor productivity, can be computed over some interval by taking the ratio of the number of cycles to the number of instructions graduated" and page 2 col 2 lines "monitoring miss rates of the shared cache of a standard node would enable the system to either schedule only one thread per module or to possibly identify "compatible" threads to co-schedule.") monitoring is checking if threads are compatible and ready to execute.

Claims 17-20, 23,24, 32 and 33-36, 39,40 and 48 are system and computer program product claims of claims 1-4, 7, 8 and 16 above. They are therefore rejected under the same rational.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 6, 13, 15, 21, 22, 29, 31, 37, 38, 45 and 47 are rejected under 35 U.S.C. 103(a) being unpatentable over "Using Performance Reflection in Systems Software" by Robert Fowler (Fowler) in view of Chrysos et al.(Chrysos) US Patent 6,549,930.

As per claim 5 Fowler discloses all the elements of claim 5 except, ***writing a first identifier corresponding to the first thread and the CPI value to a compatibility list that corresponds to the second thread.***

On the other hand Chrysos discloses:

- writing a first identifier corresponding to the first thread and the CPI value to a compatibility list that corresponds to the second thread (col 6 lines 26-30, "The profile registers can record many useful facts about an instruction's execution. Example performance information can include: the number of cycles the selected instruction spent in each stage of an execution pipeline" and lines 63-65, "Accordingly, in order to measure useful concurrency, a technique called "pair-wise sampling" is provided. The basic idea is to implement a nested form of sampling. Here, a window of instructions that may execute concurrently with a first profiled

instruction is dynamically defined.") profiling register is identifying and using the profile value to pair instructions or combination of threads.

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Chrysos into the method of Fowler to have identifier to identify compatibility between 1st and 2nd thread. The modification would have been obvious because one of the ordinary skills of the art would want to identification between thread for better tracking and scheduling.

As per claim 6, the rejection of claim 5 is incorporated and further Chrysos discloses:

- wherein the writing is performed in response to identifying an empty field in the second thread's compatibility list (col 12 lines 23-24, "an instruction that is being profiled has a "profile" bit asserted") a profile bit in a instruction is the identification field.

As per claim 13, the rejection of claim 12 is incorporated and further Chrysos discloses:

- wherein the thread that is about to complete and the compatible thread are listed in a first run queue and wherein the thread that is not about to complete is listed in a second run queue (col 9 lines 58-61, "fetched instructions are ordered by an issue unit 230. The issue unit 230 includes an issue queue having a head-of-the-queue entry 231 for the next instruction to be executed" and col 11 lines 33, "Instructions then proceed to the instruction queue 230 where they wait for two events before executing")issue queue is the first run queue and instruction queue is the 2nd queue.

The claim limitation of claim 15 has the same limitation of claim 13 above. Therefore they are rejected under the same rational.

Claims 21, 22, 29, 31 and 37, 38, 45, 47 are system and computer program product claims of claims 5, 6, 13 and 15 above. They are therefore rejected under the same rational.

9. Claims 9, 12, 14, 25, 28, 30, 41, 44 and 46 are rejected under 35 U.S.C. 103(a) being unpatentable over "Using Performance Reflection in Systems Software" by Robert Fowler (Fowler) in view of Walker et al. (Walker) US Patent 5,963,911.

As per claim 9 Fowler discloses all the elements of claim 9 except, ***writing a first identifier corresponding to the first thread to a compatibility list corresponding to the second thread.***

On the other hand Walker discloses:

- writing a first identifier corresponding to the first thread to a compatibility list corresponding to the second thread, wherein the compatibility list stores a plurality of thread identifiers compatible with the second thread (col 2 lines 47, "storing parameters relating to the jobs" and col 2 lines 6-12, "determining the combination which produces the smallest total projected cost. The method may be operated such that when a resource becomes available the steps described above are performed, the available resource then being assigned to the job which is associated with it in the smallest cost combination identified by the above procedure.")

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Walker into the method of Fowler to identify

first identifier corresponding to the first thread to a compatibility list corresponding to the second thread. The modification would have been obvious because one of the ordinary skills of the art would want to have identification in a compatible thread list to keep track and have a list of compatible list for execution.

As per claim 12, the rejection of claim 1 is incorporated and further Walker discloses:

- sensing that either the first thread or the second thread is about to complete; scheduling a new thread to execute, the scheduling comprising: identifying a compatible thread, the compatible thread being compatible to the tread that is not about to complete; determining whether the compatible thread is ready to execute; and dispatching the compatible thread to execute on the SMT processor (col 3 lines 15-16, "to determine the combination which produces the smallest total projected cost" and lines 53-56, "In a preferred arrangement only resources which have completed their current job are informed of the next job allocated to them.")

As per claim 14 Fowler discloses all the elements of claim 14 except, ***sensing that a completing thread that is about to complete execution..***

On the other hand Walker discloses:

- sensing that a completing thread that is about to complete execution on the SMT processor; identifying a running thread that is still executing on the SMT processor; checking a list of one or more compatible threads, wherein the compatible threads are compatible with the running thread; determining that one of the compatible threads is ready to execute; and

dispatching the determined thread to execute on the SMT processor. (col 3 lines 15-16, "to determine the combination which produces the smallest total projected cost" and lines 53-56, "In a preferred arrangement only resources which have completed their current job are informed of the next job allocated to them.")

Claims 25, 28, 30 and 41, 44, 46 are system and computer program product claims of claims 9, 12 and 14 above. They are therefore rejected under the same rational.

10. Claims 10, 11, 26, 27, 42 and 43 are rejected under 35 U.S.C. 103(a) being unpatentable over "Using Performance Reflection in Systems Software" by Robert Fowler (Fowler) in view of Walker et al. (Walker) US Patent 5,963,911 and in view of "TEST: A Tracer for Extracting Speculative Threads"(Tracer).

As per claim 10 Fowler discloses all the elements of claim 9 except, ***writing a timestamp corresponding to the first identifier.***

On the other hand Tracer discloses:

- writing a timestamp corresponding to the first identifier, the timestamp indicating a time at which the time interval occurred, wherein each of the plurality of thread identifiers also include a plurality of timestamps indicating when each of the threads executed with the second thread. (page 4 sec 4.2 lines 4-7, "analysis relies on the notion of event timestamps, or the time when an event occurs. Timestamps from different events are compared against each other to compute specific statistics.")

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Walker into the combined method of Fowler and Walker to have time stamp to the identified thread. The modification would have been obvious because one of the ordinary skills of the art would want to have timestamp on the thread for evaluation purpose and to have compatibility status at any time of the system for better scheduling.

As per claim 11, the rejection of claim 10 is incorporated and further Walker discloses:

- reading the entries corresponding to each of the threads listed in the compatibility lists; comparing the timestamps listed in the compatibility list with a current time; determining, based on the comparison, whether the entry associated with the timestamp is stale; and removing the entry in response to determining that it is a stale entry. (page 5 sec 4.2.1 lines 5-13, "A store timestamp is recorded on a memory or local variable store, and retrieved on a subsequent load to the same address. The store timestamp is checked against thread start timestamps to determine if an inter-thread dependency arc exists to the previous thread (t-1), or an earlier thread (< t-1).")

Claims 26, 27 and 42, 43 are system and computer program product claims of claims 10 and 11 above. They are therefore rejected under the same rational.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

TITLE: Resource Allocation, US Patent No. 5,963,911.

TITLE: TEST: A Tracer for Extracting Speculative Threads; Michael Chen, Kunle Olukotun; Code Generation and Optimization, March 2003.

TITLE: Using Performance Reflection in Systems Software; Robert Fowler, Alan Cox, Sameh Elnikety,Willy Zwaenepoel; Proceedings of HotOS IX: The 9th Workshop on Hot Topics in Operating Systems; May 2003

TITLE: Method and scheduling thread in a multithreaded processor, US 6,549,930 B1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah-Al Kawsar whose telephone number is 571-270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-270-1392. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

Chameli Das

CHAMELI DAS
SUPERVISORY PATENT EXAMINER

6/25/07.